

FAB NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE NOTED.
2. THE PWB SHALL BE FABRICATED TO IPC-6012, CLASS 2 AND WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2. CURRENT REVISIONS.
3. BOARD MATERIAL SHALL BE 180 Tg/350 Td ISOLA FR-370HR OR EQUIVALENT, ROHS COMPLIANT AND LEAD FREE ASSEMBLY CAPABLE. BOARD MATERIAL SHALL MEET OR EXCEED IPC-4101B. COLOR: NATURAL.
4. BOARD MATERIAL & CONSTRUCTION TO BE U.L. APPROVED AND MARKED ON THE FINISHED BOARD.
5. MINIMUM COPPER WALL THICKNESS OF PLATED-THRU HOLES TO BE .001 INCH, WITH A MINIMUM ANNULAR RING OF .002 INCH.
6. OVERALL BOARD THICKNESS TO BE .062 +/- 10% AND APPLIES AFTER ALL LAMINATION AND PLATING PROCESSES, MEASURED FROM COPPER TO COPPER.
7. MAX. WARP & TWIST TO BE .0075 INCHES PER INCH.
8. BOARD MUST BE ELECTRICALLY TESTED USING SUPPLIED IPC-D-356 NETLIST.
9. ALL VIAS TO HAVE SOLDERMASK.

FINISHED AS SMOOTH WALL BY VEDOR.

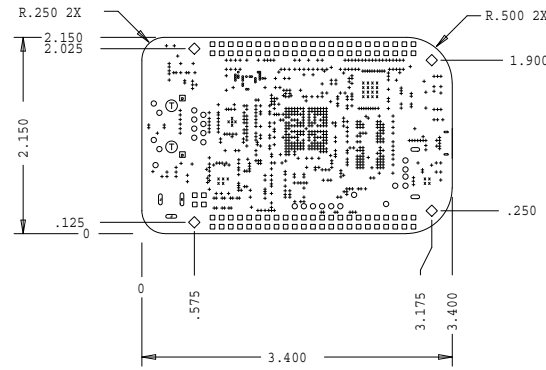
PROCESS NOTES:

1. PLATE ALL EXPOSED AREAS WITH ELECTROLESS IMMERSION GOLD, NICKEL 150 MICROINCHES THK MIN GOLD 5-15 MICROINCHES THK MIN.
2. APPLY LPI SOLDERMASK OVER BARE COPPER (SMOBC), COLOR: BLACK. SOLDERMASK SHALL CONFIRM TO IPC-SM-840. CLASS H. CURRENT REV.
3. SOLDERMASK ARTWORK HAS ZERO (0) OVERSIZED PADS. FABRICATION VENDOR IS ALLOWED TO ADJUST THE COMPONENT SOLDERMASK PADS TO MEET THEIR TOOLING REQUIREMENTS.
4. APPLY LPI SILKSCREEN OR EQUIVALENT PER THE ARTWORK. COLOR: WHITE.

DRILL CHART: TOP TO BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	6.0	+3.0/-3.0	PLATED	27
•	8.0	+3.0/-3.0	PLATED	794
•	12.0	+3.0/-3.0	PLATED	30
○	30.0	+3.0/-3.0	PLATED	96
○	40.0	+3.0/-3.0	PLATED	26
■	63.0	+3.0/-3.0	PLATED	2
◇	125.0	+3.0/-3.0	PLATED	4
⊙	128.0	+5.0/-5.0	NON-PLATED	2
-	50.0x15.0	+3.0/-3.0	PLATED	2
○	95.0x40.0	+3.0/-3.0	PLATED	2
⊗	120.0x40.0	+3.0/-3.0	PLATED	1
⊗	120.0x40.0	+3.0/-3.0	PLATED	1
⊗	140.0x40.0	+3.0/-3.0	PLATED	1

LAYER STACK-UP - ALL DIMENSIONS IN INCHES

LAYER#	COPPER WEIGHT (oz)	50ohm SINGLE ENDED IMPEDANCE CONTROL +/- 10%			90ohm DIFFERENTIAL IMPEDANCE CONTROL +/- 10%			100ohm DIFFERENTIAL IMPEDANCE CONTROL +/- 10%		
		TRACE WIDTH	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE	
LAYER 1 - PRIMARY SIDE - SIGNAL	HALF-PLATING	4.75	4.5/6.5	3.75/7.25						
LAYER 2 - GROUND PLANE	1									
LAYER 3 - SIGNAL	1	5.25	5.0/7.0	4.00/8.00						
LAYER 4 - SIGNAL	1	5.25	5.0/7.0	4.00/8.00						
LAYER 5 - SPLIT POWER PLANE	1									
LAYER 6 - SECONDARY SIDE - SIGNAL	HALF-PLATING	4.75	4.5/6.5	3.75/7.25						



APPROVED				CIRCUITCO.	
CHECKED					
DRAFTING		CalCad			
DATE	04/02/13	ENGR		FABRICATION DRAWING, BeagleBone Black	
DESIGN ENGR		TOLERANCES UNLESS OTHERWISE SPECIFIED			
PROJECT ENGR		X.XX ± 0.01			
ENGR MGR		X.XXX ± 0.005			
NEXT ASSEMBLY		DO NOT SCALE DRAWING		SCALE	NONE
				SHEET	1 OF 1
				PCB REV	B4
				SIZE	D