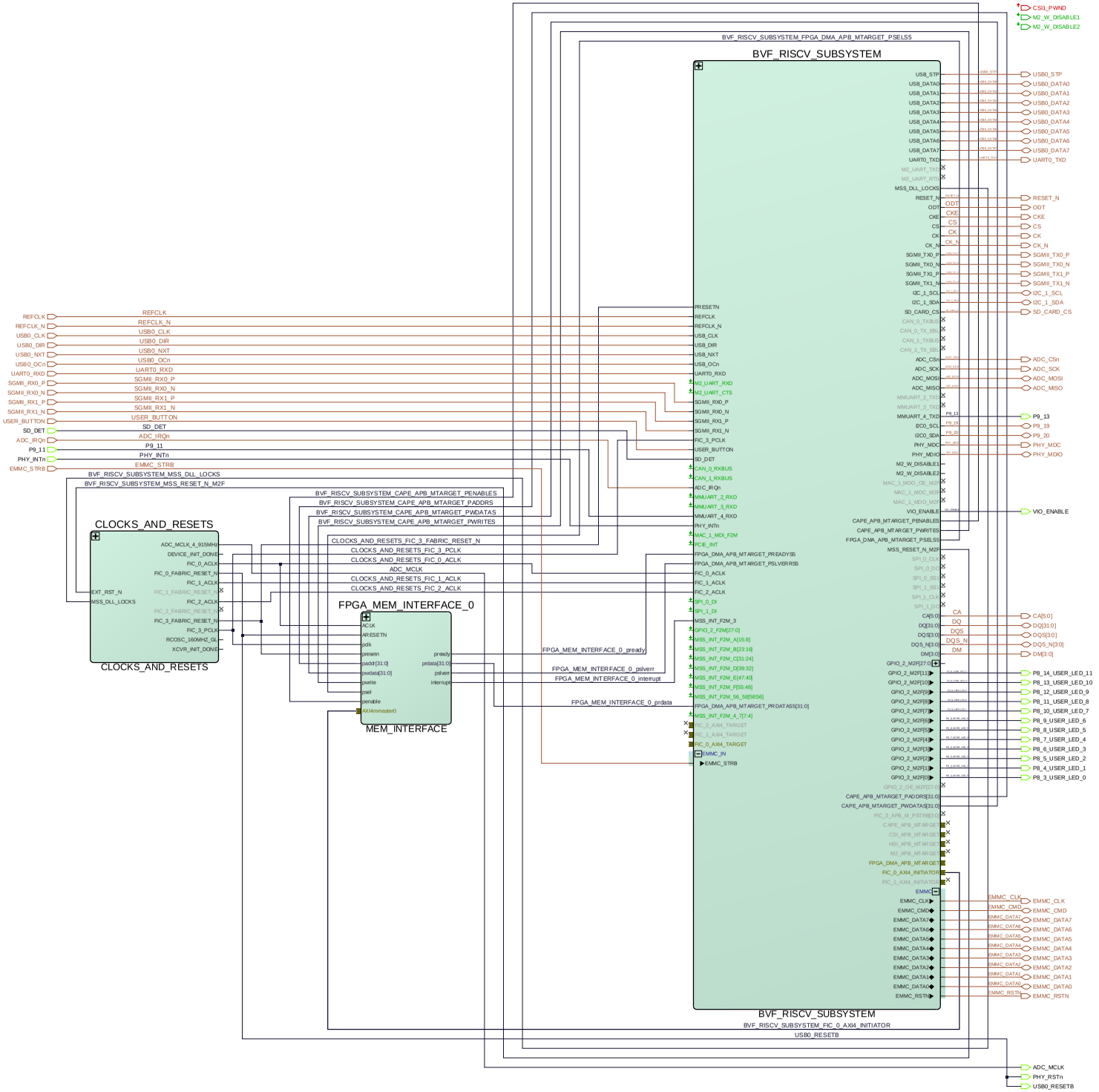
BVF_RISCV_SUBSYSTEM
CLOCKS_AND_RESETS
FPGA_MEM_INTERFACE_0
MEM_INTERFACE
REFCLK
REFCLK_N
USB0_CLK
USB0_DIR
USB0_NXT
USB0_OCn
UART0_RXD
SGMII_RX0_P
SGMII_RX0_N
SGMII_RX1_P
SGMII_RX1_N
USER_BUTTON
SD_DET
ADC_IRQn
P9_11
PHY_INTn
EMMC_STRB
BVF_RISCV_SUBSYSTEM_MSS_DLL_LOCKS
BVF_RISCV_SUBSYSTEM_MSS_RESET_N_M2F
BVF_RISCV_SUBSYSTEM_CAPE_APB_MTARGET_PENABLES
BVF_RISCV_SUBSYSTEM_CAPE_APB_MTARGET_PADDRS
BVF_RISCV_SUBSYSTEM_CAPE_APB_MTARGET_PWDATAS
BVF_RISCV_SUBSYSTEM_CAPE_APB_MTARGET_PWRITES
CLOCKS_AND_RESETS_FIC_3_FABRIC_RESET_N
CLOCKS_AND_RESETS_FIC_3_PCLK
CLOCKS_AND_RESETS_FIC_0_ACLK
ADC_MCLK
CLOCKS_AND_RESETS_FIC_1_ACLK
CLOCKS_AND_RESETS_FIC_2_ACLK
FPGA_MEM_INTERFACE_0_pready
FPGA_MEM_INTERFACE_0_psilverr
FPGA_MEM_INTERFACE_0_interrupt
FPGA_MEM_INTERFACE_0_prdata
BVF_RISCV_SUBSYSTEM_FPGA_DMA_APB_MTARGET_PSELS5
BVF_RISCV_SUBSYSTEM_FIC_0_AXI4_INITIATOR
USB0_RESETB
CSI1_PWND
M2_W_DISABLE1
M2_W_DISABLE2
USB0_STP
USB0_DATA0
USB0_DATA1
USB0_DATA2
USB0_DATA3
USB0_DATA4
USB0_DATA5
USB0_DATA6
USB0_DATA7
UART0_TXD
RESET_N
ODT
CKE
CS
CK
CK_N
SGMII_TX0_P
SGMII_TX0_N
SGMII_TX1_P
SGMII_TX1_N
I2C_1_SCL
I2C_1_SDA
SD_CARD_CS
ADC_CSn
ADC_SCK
ADC_MOSI
ADC_MISO
P9_13
P9_19
P9_20
PHY_MDC
PHY_MDIO
VIO_ENABLE
CA[5:0]
DQ[31:0]
DQS[3:0]
DQS_N[3:0]
DM[3:0]
P8_14_USER_LED_11
P8_13_USER_LED_10
P8_12_USER_LED_9
P8_11_USER_LED_8
P8_10_USER_LED_7
P8_9_USER_LED_6
P8_8_USER_LED_5
P8_7_USER_LED_4
P8_6_USER_LED_3
P8_5_USER_LED_2
P8_4_USER_LED_1
P8_3_USER_LED_0
EMMC_CLK
EMMC_CMD
EMMC_DATA7
EMMC_DATA6
EMMC_DATA5
EMMC_DATA4
EMMC_DATA3
EMMC_DATA2
EMMC_DATA1
EMMC_DATA0
EMMC_RSTN
ADC_MCLK
PHY_RSTn
USB0_RESETB