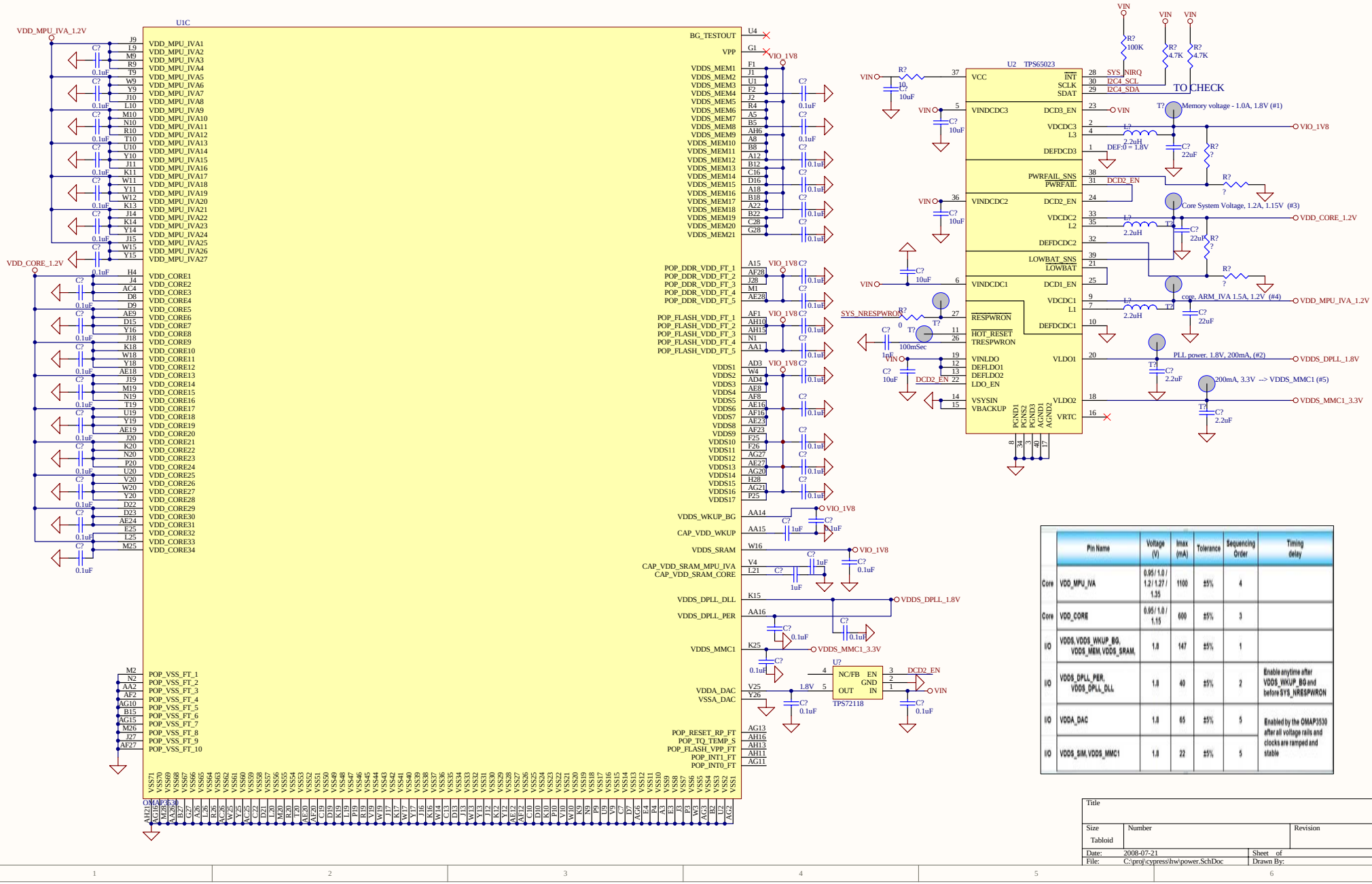

	Pin Name	Voltage (V)	Imax (mA)	Tolerance	Sequencing Order	Timing delay
Core	VDD_MPU_IVA	0.95 / 1.0 / 1.2 / 1.27 / 1.35	1100	±5%	4	
Core	VDD_CORE	0.95 / 1.0 / 1.15	600	±5%	3	
I/O	VDD8, VDD8_WKUP_BG, VDD8_MEM, VDD8_SRAM,	1.8	147	±5%	1	
I/O	VDD8_DPLL_PER, VDD8_DPLL_DLL	1.8	40	±5%	2	Enable anytime after VDD8_WKUP_BG and before SYS_NRESPWRON
I/O	VDDA_DAC	1.8	65	±5%	5	Enabled by the OMAP3530 after all voltage rails and clocks are ramped and stable
I/O	VDD8_SIM, VDD8_MMC1	1.8	22	±5%	5	